IN THE CLAIMS

1. Cancelled.

2. Cancelled.

3. Cancelled.

4. (Previously presented) A shift bar circuit comprising

one or more inputs for receiving one or more independent binary input signals;

a circuit for converting said binary signals into a state signal having one unique bit and representative of the input binary signals;

a restoration circuit connected to the state signal for restoring the state signal to a desired voltage level;

a carry circuit coupled to the outputs of the shift bar circuit for generating an output corresponding to carry bits generated by the shift bar circuit; and a second or more shift bar circuits cascaded together to produce a modulo sum and one or more carry bits; an encoder circuit for converting the shift level modulo sum signal into a binary sum output signal.

5. (Original) The shift bar circuit of claim 4 further comprising a full adder coupled to the output the encoder circuit.

6. (Amended) A shift switch parallel counter comprising a converter for converting input binary signals into state signals at an original level, a compressor for receiving the state signals from the converter and having at least one shift bar circuit for adding a binary input to the state signals, an encoder for encoding the state signals into sum and carry bits, and a restoration circuit for restoring the state signals from the encoder into their original levels and providing a carry bit~~, and an encoder for encoding the state signals into receive and carry bits.~~

7. (Previously presented) The shift switch parallel counter of claim 6 wherein the restoration circuit of the compressor comprises a shift bar circuit for receiving one binary input signal of weight 1 and one shift bar binary input signal of weight 1, and producing a binary sum bit of weight 1 and a binary carry bit of weight 2.

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8. (Previously presented) The shift switch parallel counter circuit of claim 6 wherein the compressor comprises two or more second shift bar circuit cascaded to the first shift bar circuit and each cascaded shift bar circuit receiving the state signal output of the prior shift bar circuit and adding a binary input the prior state signal.

9. (Previously presented) The shift switch parallel counter circuit of claim 8 comprising at least a third shift bar circuit in the compressor for compressing three inputs bits into two output bits.

10. (Original) The shift switch parallel counter circuit of claim 8 receiving one binary input signal of weight 1, three shift bar binary input signals of weight 1, and a binary input carry signal of weight 1, and producing a binary sum bit, a binary carry bit of weight 2, and one binary output signal of weight 2 corresponding to an in-stage carry bit generated by the shift bar circuits.

11. (Original) The shift switch parallel counter circuit of claim 10 comprising a shift switch parallel counter compressing four inputs bits into two output bits.

12. (Original) A compressor circuit comprising: two or more shift bar circuits cascaded with each other, a restoration circuit coupled to the output of the last shift bar circuit; a carry circuit coupled to the shift bar circuits; an encoder circuit coupled to the output of the last shift bar circuit; wherein each shift bar circuit having a plurality of state signal lines and a binary input signal connected to all of the state signal lines for shifting the state signals in accordance with the value of the shift bar input binary signal to create a modulo sum and carry bits in accordance with the combination of the independent input binary signals and the bar circuit input binary signals, the state signal lines of one of the shift bar circuits coupled to the output of the input converter circuit for receiving the first state signal, said restoration circuit coupled to the output of the last shift bar circuit for restoring the signal level of the state signals to their input levels, said carry circuit coupled to the outputs of each shift bar circuit for generating an output corresponding to carry bits generated by the shift bar circuits, said encoder circuit for converting the shift level modulo sum signal into a binary sum output signal.

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13. (Original) A compressor circuit comprising: an input converter circuit, two or more shift bar circuits cascaded with each other, a restoration circuit, a carry circuit, and an encoder circuit, said input converter circuit for receiving one or more independent binary input signals, converting said binary signals into a first state signal having one unique bit and representative of the input binary signals, each shift bar circuit having a plurality of state signal lines and a binary input signal connected to all of the state signal lines for shifting the state signals in accordance with the value of the shift bar input binary signal to create a modulo sum and carry bits in accordance with the combination of the independent input binary signals and the bar circuit input binary signals, the state signal lines of one of the shift bar circuits coupled to the output of the input converter circuit for receiving the first state signal, said restoration circuit coupled to the output of the last shift bar circuits for restoring the signal level of the state signals to their input levels, said carry circuit coupled to the outputs of each shift bar circuit for generating an output corresponding to carry bits generated by the shift bar circuits, said encoder circuit for converting the shift level modulo sum signal into a binary sum output signal.

14. (Original) A shift switch parallel counter circuit for counting binary input signals and producing a sum signal and a plurality of carry signals, comprising: an input converter circuit, two or more shift bar circuits cascaded with each other, a restoration circuit, a carry circuit, an encoder circuit, and a full adder circuit, said input converter circuit for receiving one or more independent binary input signals, converting said binary signals into a first state signal having one unique bit and representative of the input binary signals, each shift bar circuit having a plurality of state signal lines and a binary input signal connected to all of the state signal lines for shifting the state signals in accordance with the value of the shift bar input binary signal to create a modulo sum and carry bits in accordance with the combination of the independent input binary signals and the bar circuit input binary signals, the state signal lines of one of the shift bar circuits coupled to the output of the input converter circuit for receiving the first state signal, said restoration circuit coupled to the output of the last shift bar circuits for restoring the signal level of the state signals to their input levels, said carry circuit coupled to the outputs of each shift bar circuit for generating an output corresponding to carry bits generated by the shift bar circuits, said encoder

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circuit for converting the shift level modulo sum signal into a binary sum output signal, said full adder circuit for adding one or more late-arriving binary signals to the binary sum output signal to produce a binary sum bit and a binary carry bit.

15. (Original) The shift switch parallel counter circuit of claim 14 receiving four binary input signals of weight 1, one shift bar binary input signal of weight 2, and two binary input carry signals of weight 2, and producing a binary sum bit of weight 2, a binary carry bit of weight 4, and two binary output signals of weight 1 and weight 4 respectively corresponding to in-stage carry bits generated by the shift bar circuits.

16. (Original) The shift switch parallel counter circuit of claim 15 comprising a shift switch parallel counter compressing five inputs bits into two output bits.

17. (Original) The shift switch parallel counter circuit of claim 14 receiving three binary input signals of weight 1, two shift bar binary input signal of weight 1, one shift bar binary input signal of weight 2, and two binary input carry signals of weight 2, and producing a binary sum bit of weight 2, a binary carry bit of weight 4, and two binary output signals of weight 1 and 4 respectively corresponding to in-stage carry bits generated by the shift bar circuits.

18. (Original) The shift switch parallel counter circuit of claim 17 comprising a shift switch parallel counter compressing six inputs bits into two output bits.

19. (Original) The shift switch parallel counter circuit of claim 14 receiving five binary input signals of weight 1, two shift bar binary input signals of weight 1, and two binary input carry signals of weight 2, and producing a binary sum bit of weight 2, a binary carry bit of weight 4, and two binary output signals of weights 1 and 4 respectively corresponding to in-stage carry bits generated by the shift bar circuits.

20. (Original) The shift switch parallel counter circuit of claim 19 comprising a shift switch parallel counter compressing six inputs bits into two output bits and a shift switch parallel counter compressing three input bits into two output bits.

21. (Original) The shift switch parallel counter circuit of claim 14 receiving five

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binary input signals of weight 1, three shift bar binary input signals of weight 1, and two binary input carry signals of weight 2, and producing a binary sum bit of weight 2, a binary carry bit of weight 4, and two binary output signals of weight 1 and two binary output signals of weight 4 corresponding to in-stage carry bits generated by the shift bar circuits.

22. (Original) The shift switch parallel counter circuit of claim 21 comprising a shift switch parallel counter compressing six inputs bits into two output bits and two shift switch parallel counters each compressing three input bits into two output bits.

23. (Original) The shift switch parallel counter circuit of claim 14 receiving five binary input signals of weight 1, four shift bar binary input signals of weight 1, one binary input carry signal of weight 1, and two binary input carry signals of weight 2, and producing a binary sum bit of weight 2, a binary carry bit of weight 4, and two binary output signals of weight 1, one binary output signal of weight 2, and two binary output signals of weight 4 corresponding to in-stage carry bits generated by the shift bar circuits.

24. (Original) The shift switch parallel counter circuit of claim 23 comprising a shift switch parallel counter compressing six inputs bits into two output bits, a shift switch parallel counter compressing four input bits into two output bits, and a shift switch parallel counter compressing three input bits into two output bits.

25. (Previously presented) The shift switch parallel counter circuit of claim 14 receiving three binary input signals of weight 1, one shift bar binary input signal of weight 1, one shift bar binary input signal of weight 2, and two binary input carry signals of weight 2, and producing a binary sum bit, a binary carry bit, and two binary output signals of weight and respectively corresponding to in-stage carry bits generated by the shift bar circuits.

26. (Original) The shift switch parallel counter circuit of claim 25 comprising a shift switch parallel counter compressing six inputs bits into two output bits.

27. Cancelled.

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28. (Previously presented) A partial product matrix reduction circuit comprising: two or more stages of parallel counters, each stage reducing a number of input bits into a smaller number of output bits and the last stage reducing the number of its input bits to two output bits wherein the parallel counters comprise interconnected cascaded shift switch parallel counter circuits, each shift switch parallel counter circuit comprising: an input converter circuit, two or more shift bar circuits cascaded with each other, a restoration circuit, a carry circuit, an encoder circuit, and a full adder circuit, said input converter circuit for receiving one or more independent binary input signals, converting said binary signals into a first state signal having one unique bit and representative of the input binary signals, each shift bar circuit having a plurality of state signal lines and a binary input signal connected to all of the state signal lines for shifting the state signals in accordance with the value of the shift bar input binary signal to create a modulo sum and carry bits in accordance with the combination of the independent input binary signals and the bar circuit input binary signals, the state signal lines of one of the shift bar circuits coupled to the output of the input converter circuit for receiving the first state signal, said restoration circuit coupled to the output of the last shift bar circuits for restoring the signal level of the state signals to their input levels, said carry circuit coupled to the outputs of each shift bar circuit for generating an output corresponding to carry bits generated by the shift bar circuits, said encoder circuit for converting the shift level modulo sum signal into a binary sum output signal, said full adder circuit for adding one or more late-arriving binary signals to the binary sum output signal to produce a binary sum bit and a binary carry bit.

29. (Previously presented) The partial product reduction matrix of claim 28 further comprising a final adder circuit.

30. (Previously presented) The partial product reduction matrix of claim 28 wherein the first, second, and output numbers are integers expressed in binary form.

31. (Original) The partial product reduction matrix of claim 30 wherein the plurality of interconnected cascaded shift switch parallel counter circuits of the matrix reduction circuits comprises: in a first stage, a plurality of shift switch parallel

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counters each compressing four inputs bits into two output bits and a plurality of shift switch parallel counters each compressing six inputs bits into two output bits, and in a second stage, a plurality of shift switch parallel counters each compressing eight inputs bits into two output bits.

32. (Original) The partial product reduction matrix of claim 29 wherein the first, second, and output numbers are integers expressed in binary form, and Booth recoding is used to encode the first and second numbers for multiplication.

33. (Original) The partial product reduction matrix of claim 35 wherein the plurality of interconnected cascaded shift switch parallel counter circuits of the matrix reduction circuits comprises: in a first stage, a plurality of shift switch parallel counters each compressing eight inputs bits into two output bits, and in a second stage, a plurality of shift switch parallel counters each compressing nine inputs bits into two output bits.

34. (Previously presented) The partial product reduction matrix of claim 28 wherein the first, second, and output numbers are floating-point numbers expressed in binary form.

35. (Previously presented) The partial product reduction matrix of claim 34 wherein the plurality of interconnected cascaded shift switch parallel counter circuits of the matrix reduction circuits comprises: in a first stage, a plurality of shift switch parallel counters each compressing seven inputs bits into two output bits and a plurality of shift switch parallel counters each compressing eight inputs bits into two output bits, and in a second stage, a plurality of shift switch parallel counters each compressing four inputs bits into two output bits, and a plurality of shift switch parallel counters each compressing six inputs bits into two output bits.

36. (Previously presented) The partial product reduction matrix of claim 29 wherein the first, second, and output numbers are integers expressed in binary form.

37. (Previously presented) The partial product reduction matrix of claim 36 wherein the plurality of interconnected cascaded shift switch parallel counter circuits

of the matrix reduction circuits comprises: in a first stage, a plurality of shift switch parallel counters each compressing nine inputs bits into two output bits and a plurality of shift switch parallel counters each compressing two inputs bits into two output bits, and in a second stage, a plurality of shift switch parallel counters each compressing four inputs bits into two output bits and a plurality of shift switch parallel counters each compressing six inputs bits into two output bits.

38. (Original) A small eight-by-eight shift switch parallel multiplier circuit for multiplying two eight-bit numbers, comprising a plurality of shift switch parallel counters, each shift switch parallel counter further comprising: an input converter circuit, two or more shift bar circuits cascaded with each other, a restoration circuit, a carry circuit, an encoder circuit, and a full adder circuit, said input converter circuit for receiving one or more independent binary input signals, converting said binary signals into a first state signal having one unique bit and representative of the input binary signals, each shift bar circuit having a plurality of state signal lines and a binary input signal connected to all of the state signal lines for shifting the state signals in accordance with the value of the shift bar input binary signal to create a modulo sum and carry bits in accordance with the combination of the independent input binary signals and the bar circuit input binary signals, the state signal lines of one of the shift bar circuits coupled to the output of the input converter circuit for receiving the first state signal, said restoration circuit coupled to the output of the last shift bar circuits for restoring the signal level of the state signals to their input levels, said carry circuit coupled to the outputs of each shift bar circuit for generating an output corresponding to carry bits generated by the shift bar circuits, said encoder circuit for converting the shift level modulo sum signal into a binary sum output signal, said full adder circuit for adding one or more late-arriving binary signals to the binary sum output signal to produce a binary sum bit and a binary carry bit.

39. (Original) A small eight-by-eight shift switch parallel multiplier circuit for multiplying two eight-bit numbers, comprising: a plurality of shift switch parallel counters compressing six inputs bits into two output bits, a plurality of shift switch parallel counters compressing three inputs bits into two output bits, a plurality of shift switch parallel counters compressing two inputs bits into two output bits, a plurality of shift switch parallel counters compressing four inputs bits into three output bits.

40. (Original) The parallel multiplier of claim 39 comprising a composite sixteen-by-sixteen shift switch parallel multiplier circuit for multiplying two sixteen-bit numbers, comprising a plurality of the small eight-by-eight shift switch parallel multiplier circuits of claim 39.

41. (Original) The parallel multiplier of claim 40 comprising a composite thirty-two-by-thirty-two shift switch parallel multiplier circuit for multiplying two thirty-two-bit numbers, comprising a plurality of the composite sixteen-by-sixteen shift switch parallel multiplier circuits.

42. (Original) A composite sixty-four-by-sixty-four shift switch parallel multiplier circuit for multiplying two sixty-four-bit numbers, comprising a plurality of the composite thirty-two-by-thirty-two shift switch parallel multiplier circuits of claim 41.

43. (Original) A small shift switch parallel multiplier circuit for multiplying two binary numbers, comprising a plurality of shift switch parallel counters each further comprising a compressor circuit, each said compressor circuit further comprising: two or more shift bar circuits cascaded with each other, a restoration circuit, a carry circuit, and an encoder circuit, each shift bar circuit having a plurality of state signal lines and a binary input signal connected to all of the state signal lines for shifting the state signals in accordance with the value of the shift bar input binary signal to create a modulo sum and carry bits in accordance with the combination of the independent input binary signals and the bar circuit input binary signals, the state signal lines of one of the shift bar circuits coupled to the output of the input converter circuit for receiving the first state signal, said restoration circuit coupled to the output of the last shift bar circuit for restoring the signal level of the state signals to their input levels, said carry circuit coupled to the outputs of each shift bar circuit for generating an output corresponding to carry bits generated by the shift bar circuits, said encoder circuit for converting the shift level modulo sum signal into a binary sum output signal.

44. (Original) A composite shift switch parallel multiplier circuit for multiplying two binary numbers, comprising a plurality of the small shift switch parallel multiplier

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circuits of claim 43.

45. (Original) A composite shift switch parallel multiplier circuit for multiplying two binary numbers, comprising a plurality of the composite shift switch parallel multiplier circuits of claim 44.

46. (Currently amended) ~~A reconfigurable matrix multiplier circuit for multiplying two mathematical matrices, comprising: an input network of multipliers connected to input bit signal lines, for linking each input line to a plurality of configuration control switches, a first output network of adders and a second output network of accumulators, said adder and accumulator networks connected to the configuration control switches a plurality of configuration control switches connected to the reconfigurable input network and to the output networks for selecting among multiple input bit signal lines, and connecting the outputs of the multipliers to one of two output networks.~~

A reconfigurable matrix multiplier circuit for multiplying two mathematical matrices, comprising:

an input network of multipliers connected to input bit signal lines for generating partial product output signals representative of the partial product of two multiplied mathematical matrices;

a first output network of adders and a second output network of accumulators; and

a plurality of configuration control switches coupled to the multipliers and to output networks and selectively operable between first and second state to connect the partial product output signals of the multipliers to the output network of adders when the control switches are in their first state and for connecting the partial product output signals of the multipliers to the output network of accumulators when the control switches are in their second state.

47. (Currently amended) ~~A composite reconfigurable matrix multiplier circuit, comprising a plurality of the reconfigurable matrix multiplier circuits of claim 46.~~

The composite reconfigurable matrix multiplier of claim 46 wherein the control switches in their first state couple the outputs of the multipliers to the output adder network for generating multiple mathematical matrix partial products and the

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control switches in their second state couple the outputs of the multipliers to the output accumulator network to generate a single mathematical matrix partial product.

48. (Original) A composite reconfigurable matrix multiplier circuit, comprising a plurality of the composite reconfigurable matrix multiplier circuits of claim 47.

49. (Original) The configuration control circuit of claim 46 ~~47~~, wherein the multipliers comprise: a plurality of multiple shift switch parallel multiplier circuits for multiplying binary numbers, each shift switch parallel multiplier circuit further comprising a compressor circuit, each said compressor circuit further comprising: two or more shift bar circuits cascaded with each other, a restoration circuit, a carry circuit, and an encoder circuit, each shift bar circuit having a plurality of state signal lines and a binary input signal connected to all of the state signal lines for shifting the state signals in accordance with the value of the shift bar input binary signal to create a modulo sum and carry bits in accordance with the combination of the independent input binary signals and the bar circuit input binary signals, the state signal lines of one of the shift bar circuits coupled to the output of the input converter circuit for receiving the first state signal, said restoration circuit coupled to the output of the last shift bar circuit for restoring the signal level of the state signals to their input levels, said carry circuit coupled to the outputs of each shift bar circuit for generating an output corresponding to carry bits generated by the shift bar circuits, said encoder circuit for converting the shift level modulo sum signal into a binary sum output signal.

50. (Original) The reconfigurable matrix multiplier circuit of claim 47, comprising a set of four smaller identical reconfigurable matrix multiplier circuits, each multiplying two 32-bit numbers or two 8-by-8 matrices.

51. (Original) The four matrix multiplier circuits of claim 50, each comprising a set of four identical matrix multiplier circuits, each multiplying two 16-bit numbers or two 4-by-4 matrices.

52. (Original) The four matrix multiplier circuits of claim 51, each comprising a set of four identical matrix multiplier circuits, each multiplying two 8-bit numbers or two 2-

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by-2 matrices.

53. (Original) The four matrix multiplier circuits of claim 53 each comprising a set of four identical matrix multiplier circuits, each multiplying two 4-bit numbers.

54. (Original) A pair of one-bit-controlled 64-bit switches enabling the matrix multiplier circuit of claim 50 to multiply either two 64-bit numbers or two 16-by-16 matrices.

55. (Original) A pair of one-bit-controlled 32-bit switches enabling the matrix multiplier circuit of claim 52 to multiply either two 32-bit numbers or two 8-by-8 matrices.

56. (Original) A pair of one-bit-controlled 16-bit switches enabling the matrix multiplier circuit of claim 52 to multiply either two 16-bit numbers or two 4-by-4 matrices.

57. (Original) A pair of one-bit-controlled 8-bit switches enabling the matrix multiplier circuit of claim 53 to multiply either two 8-bit numbers or two 2-by-2 matrices.

58. (New) A reconfigurable matrix multiplier circuit for multiplying two mathematical matrices, comprising:

an input network of multipliers connected to input bit signal lines for generating partial product output signals representative of the partial product of two multiplied mathematical matrices, wherein each multiplier comprises a converter for converting input binary signals into state signals at an original level, a compressor for receiving the state signals from the converter and has at least one shift bar circuit for adding a binary input to the state signals, an encoder for encoding the state signals into sum and carry bits, and a restoration circuit for restoring the state signals from the encoder into their original levels and providing a carry bit;

a first output network of adders and a second output network of accumulators; and

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a plurality of configuration control switches coupled to the multipliers and to output networks and selectively operable between first and second state to connect the partial product output signals of the multipliers to the output network of adders when the control switches are in their first state and for connecting the partial product output signals of the multipliers to the output network of accumulators when the control switches are in their second state.

59.(New) The reconfigurable matrix multiplier circuit of claim 58 wherein the shift bar circuit comprises:

one or more inputs for receiving one or more independent binary input signals;

a circuit for converting said binary signals into a state signal having one unique bit and representative of the input binary signals;

a restoration circuit connected to the state signal for restoring the state signal to a desired voltage level;

a carry circuit coupled to the outputs of the shift bar circuit for generating an output corresponding to carry bits generated by the shift bar circuit; and a second or more shift bar circuits cascaded together to produce a modulo sum and one or more carry bits; an encoder circuit for converting the shift level modulo sum signal into a binary sum output signal.

60.(New) The reconfigurable matrix multiplier circuit of claim 59 wherein the shift bar circuits further comprise full adders coupled to the output the encoder circuits.

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